ABSTRACT OF THE DISCLOSURE

A method for testing signals of integrated circuits (ICs). According to the invention, a first IC chip successively drives a number of test patterns one at a time. At the receiving end, a second IC chip latches in the test patterns one by one. Meanwhile, the second IC chip determines whether a currently latched test pattern is correct or not. If it is incorrect and at least an error bit occurs, depending on the type of the test patterns, the second IC chip indicates that there exists ground bounce or power bounce in a signal trace corresponding to the error bit.